CLAIMS

What is claimed is:

1. A method of converting a computer processor configuration having a k-phased pipeline into a virtual multithreaded processor, the method comprising:

dividing each pipeline phase of said processor configuration into a plurality n of sub-phases; and

creating at least one virtual pipeline within said pipeline, said virtual pipeline comprising k sub-phases.

2. A method according to claim 1 and further comprising executing a different thread within each one of said virtual pipelines.

3. A method according to claim 2 wherein said executing step comprises executing any of said threads at an effective clock rate equal to the clock rate of said k-phased pipeline.

4. A method according to claim 1 wherein said dividing step comprises:

determining a minimum cycle time T=1/f for said computer processor configuration; and

dividing each pipeline phase of said processor configuration into said plurality n of sub-phases, wherein each sub-phase has a propagation delay of less than T/n.

5. A method according to claim 2 and further comprising:

replicating the register set of said processor configuration; and

adapting said replicated register sets to simultaneously store the machine states of said threads.

6. A method according to claim 5 and further comprising:

selecting any of said threads at a clock cycle; and

activating at said clock cycle the register set that is associated with said selected thread.

7. A method according to claim 1 wherein any of said steps are applied to a single-threaded processor configuration.

8. A method according to claim 1 wherein any of said steps are applied to a multithreaded processor configuration.

9. A method according to claim 1 wherein any of said steps are applied to a given processor configuration a plurality of times for a plurality of different values of n, thereby creating a plurality of different processor configurations.

10. A method according to claim 1 wherein any of said steps are applied to a given processor configuration a plurality of times for a plurality of different values of n until a target processor performance level is achieved.

11. A method according to claim 1 wherein said dividing step comprises:

selecting a predefined target processor performance value; and

selecting a value of n being in predefined association with said predefined target processor performance level.